Modeling and Experiments of High Power Radio-Frequency Effects on Printed Circuit Boards and their Embedded Chip Elements

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Abstract— **The ability of high power microwaves (HPM) to upset electronic systems through intentional electromagnetic interference (IEMI) is well recognized. We describe our ongoing technical efforts under the Air Force Research Laboratory's (AFRL's) 3 year-long High Power Microwave Technological Electromagnetic Susceptibility with Laboratory Applications (HPMTESLA) Call 0005 program to advance the state-of-the-art in theoretical, modeling and simulation (M&S), and experimental efforts to understand and eventually predict the effects of high power Radio-Frequency (RF) and electromagnetic pulse (EMP) energy on digital electronic devices comprising printed circuit boards (PCBs) and their embedded chipsets. Through MOSIS, we have designed and fabricated several test structures and embedded digital circuits which are ubiquitous in larger digital electronic systems (such as delay line loops, ring oscillators, memory modules) utilizing modern day semiconductor process technologies of varying scales. In this presentation, we will focus on the direct injection of HPM and EMP-like waveforms into various nodes of a ring oscillator/inverter chain and discuss the observed upset phenomenology. Finally, we will describe our on-going work on building a predictive physics-based analytical model to describe the observed upset phenomenology. Such analytical models can be incorporated into circuit design simulators to gain a predictive capability towards upset of larger digital electronic systems exposed to HPM/EMP stress.**

Keywords-High Power Microwaves; EMI; EMC; Directed Energy; Electromagnetic Pulses; Integrated Circuits;

I. Introduction

It has been widely noted in the RF effects community that susceptibility to IEMI-induced upset of computer electronics can be considered at a wide spectrum of integration levels. At one end of the spectrum, the Air Force Office of Scientific Research (AFOSR) sponsored Multi-University Research Initiative (MURI)-2001 program **[1]** focused on a number of areas, including most prominently, the formulation of some physics based, analytic sub-models to explain experimentally-observed, upset phenomenology of elemental semiconductor devices (gates and transistors) due to direct IEMI injection. At the other end of the spectrum, TechFlow Scientific has just completed execution of the Air Force Research Laboratories (AFRL)-sponsored HPMTESLA Call 0006 SOO3 **[2]** study to create and develop a functional diagnostic toolkit to determine the state of a personal computer (PC) (comprising billions of elemental devices) after a free-field HPM induced upset. The research program being executed by the TechFlow Scientific team under the HPMTESLA Call 0005 solicitation is bridging a critical intellectual chasm in the HPM effects community between the physics-based explanations, commonly used for describing RF-upset in direct-IEMI-injection testing of elemental electronic components, and the more functional based explanations describing the erroneous operational behavior of PCs and higher-level systems to free field HPM exposure. By designing and fabricating test circuits, accurate physics-based analytic models can be derived to describe the observed upset phenomenology due to IEMI. These models can be subsequently scaled to higher levels of electronic circuit complexity to understand and eventually predict the observed upset phenomenology of more complex electronic systems comprising cascaded sections of these fundamental circuits.

II. Test Setup

The Test IC is designed and fabricated using the 0.5 micron ON Semiconductor process. Four circuits ubiquitous in digital electronics were implemented in this test IC. They include an inverter chain, a delay lock loop (DLL), a Static Random Access Memory (SRAM) unit, and a crystal oscillator (Figure 3). IEMI directly injected on to power or I/O lines can cause errors in each of these circuits that may disrupt the sub-circuit operation and functionality. As part of this study, we have parsed the upset phenomenology into analog domain upsets and digital domain upsets, for which we are developing analytic physics-based upset models.

III. Results

Figure 1 shows some representative results on the variation of the natural oscillation frequency of the inverter chain circuit due to an electrically fast transient injected on the power supply line, along with predictions from our analytic model.

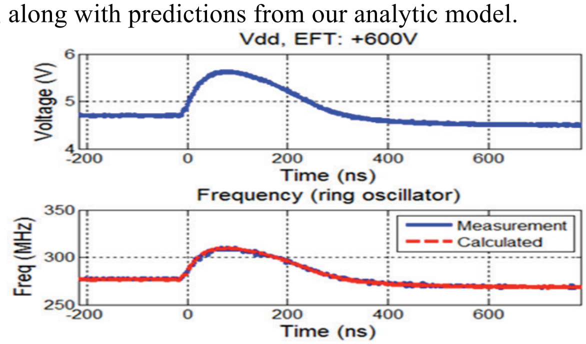

Figure 1: Variation in natural oscillation frequency due to injected EFT (blue- experiments, red- predictive model).

References

[1] www.ireap.umd.edu/MURI-2001/FinalReport-103106/MURI01FinalReport-06.pdf

[2] S.Hemmady, "RF Upset of Digital Systems", Final Technical and Scientific Report, AFRL-RDHE, Submitted Dec. 2013.